NEC

Application Note

PCB-Design for Improved EMC

Guideline for Applications with NEC Microcontroller

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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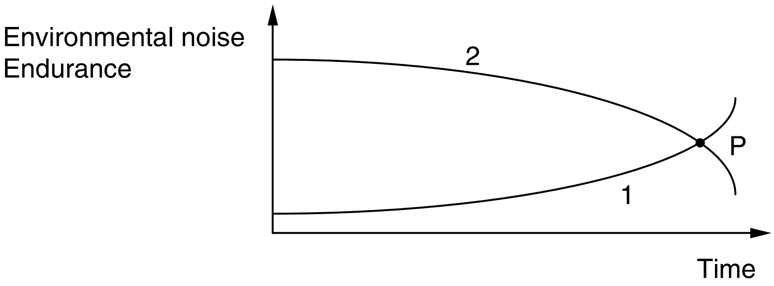
Chapter 1 Introduction

1.1 Overview

This application note is intended for hardware and/or PCB designers with a basic knowledge on PCB-design for improved EMC. Basically the background of most design rules is explained but a detailed explanation would have overloaded the structure of an application note. There is plenty of literature on the market treating system design for EMC, shielding, cabling etc. Therefore these aspects of EMC are only little handled here. This application note targets on detailed aspects of PCB design in the vicinity of NEC microcontroller.

Today with increasing tendency most automotive, consumer and industrial applications include typically one or more microcontroller. Often several electronic modules build an application system and of course several applications and/or systems may be operating vicinal. Due to the increasing number of electronic applications their density in any given environment is increasing. Therefore - as shown by curve 1 in the diagram - the environmental electromagnetic noise observed over long time at a given place rises. Functionality of electronic equipment will not be affected as long as at any given point in time its immunity is higher than the environmental electromagnetic noise. None the less unfortunately - as shown by curve 2 in the diagram - in modern systems, for example operating at higher frequencies but (due to lower power operation) having also lower switching thresholds, the noise immunity level is decreasing.

Figure 1-1: Long time environmental noise development



It is obvious that if cross point P in Figure 1-1 were to be ever reached the whole electronic market would break down. It is therefore essential for the electronic market to apply measures to improve the electromagnetic compatibility (EMC) of electronic systems and thereby continually pushing the point P towards infinity on time line.

1.2 List of Abbreviations

A	Amplitude
A_{PP}	Amplitude, peak-to-peak
A_{RMS}	Amplitude, root-mean-square
E	Amplitude of E-field
f	Frequency
l	Length, e.g. of a wire
r	Distance, e.g. from a noise source
t_F	Fall time
t_R	Rise time
Z_O	Wave impedance in far-field, constant of 377 Ω
λ	Wavelength
ω	Equals $2 \times \pi \times f$
V_{SS}	Ground potential
V_{DD}	Power supply
S	Space

Chapter 2 Background

Electromagnetic Compatibility (EMC) is the generic term for two similar issues just viewed from opposite direction. Electromagnetic Emission (EME) describes the effects when the device under Test (DUT) is the source of the noise while Electromagnetic Susceptibility (EMS) describes the effects when the DUT is the victim of the noise. As per the experience in NEC Electronics (Europe) GmbH (hereinafter called NEC EE) the main requirement on EMC related customer support is on EME issues. Therefore the descriptions in this application note mainly utilises the EME-view. Nevertheless, by just viewing from opposite direction, most measures described here are applicable for EMS as well.

2.1 Direct Semiconductor Far Field Emission

Emission may occur either radiated or conductive, the latter as noise-voltage or noise current. It is common understanding that semiconductor devices such as microcontroller are sources of EME. It is also well known that the nearer to the noise source the cheaper EME countermeasures are. As most normative radiated EME measurements are defined for the far field ($r > \lambda$) this application note shall start with a view onto the direct emission of a semiconductor device into far field.

Any current in a wire causes a far field emission. In order to get an idea about the maximum expectable semiconductor emission level the worst case emission of a straight wire (Hertz dipole) and a current loop with extreme parameters shall be calculated:

2.1.1 Straight wire (Hertz dipole)

In free space (no conductive material around) according to [1] the maximum E-field ‘E’ measured at a distance ‘r’ caused by a current ‘i’ with wavelength ‘λ’ flowing in a wire of length ‘l’ can be calculated as follows:

$$E = \frac{Z_0 \times i \times l}{2 \times r \times \lambda}$$

Example:

Measurements according to IEC61967-4 show a typical device V_{SS}-current at for example 100 MHz (λ = 3 m) of about 20 dBµA (10 µA). Assumed this current was caused by a signal on a single wire of 10 mm length and the return current flows far away (no compensation in far-field) the E-field at a distance of 10 m adds up to:

$$E = 377\,\Omega \times 10\,\mu A \times 0.01m / (2 \times 10\,m \times 3\,m) \approx 0.5\,\mu V/m \approx -6\,dB\mu V/$$

As for this approximation extreme assumptions were used the actual direct device emission should be much lower than –6 dBµV/m. Compared to common emission limits obviously the direct device emission from on-chip wiring can be neglected.

2.1.2 Current loop

According to [1] maximum E-field emission of a current 'i' with wavelength 'λ' flowing in a loop area space 'S' and measured in a distance 'r' can be calculated as follows:

$$E = \frac{Z_0 \times \pi \times i \times S}{r \times \lambda^2}$$

Example:

Assumed a current of 100 µA (40 dBµA) at 100 MHz ($\lambda = 3$ m) flows in a loop area of 1 mm^2. Measured at a distance of 10 m the resulting E-field is:

$$E = 377\ \Omega \times 3.14 \times 100\ \mu A \times 10^{-06}\ m^2 / (10\ m \times 9\ m^2) \approx\ 0{,}13\ \mu V/m \approx\ -18\ db\mu V/r$$

Again obviously the direct device emission from on-chip loop currents such as power supplies etc. can be neglected, especially as again the calculation is based on extreme assumptions.

2.2 Near Field Emission

Generally, the transition from near field to far field is related to the wavelength of the signal. In [1] the area with $r \leq 0.8\lambda$ is defined as near field while the area with $r \geq 1.2\lambda$ is defined as far field with a transition area in-between. Generally, structures leading RF-power shall be kept small enough so that their contribution to the far-field emission is low. But even then near-field emission may stimulate appropriate antenna structures nearby and by means of that remarkably contribute to the far-field emission. These system effects are not described here as this application note targets on detailed aspects of PCB design in the vicinity of NEC microcontroller.

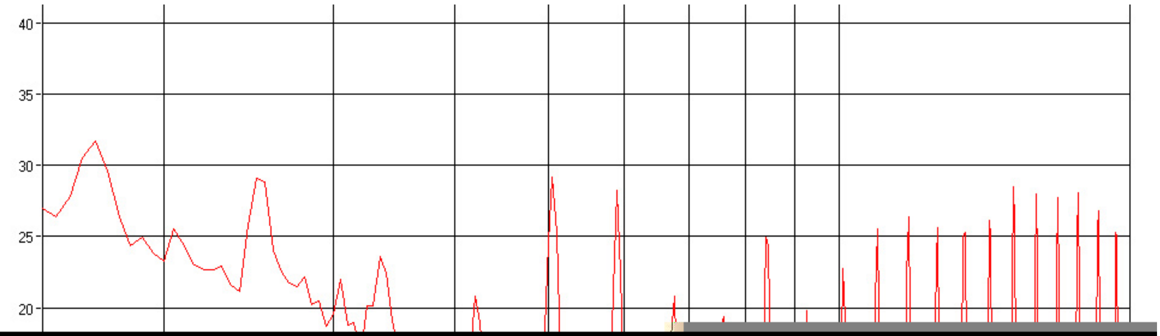
2.3 Signal Classification

2.3.1 Narrow band noise and wide band noise

According to Fourier's theory any signal can be represented by a sum of sinus- and cosinus-oscillations.

- A periodical non-sinusoidal signal, such as a clock, strobe etc. consists only of its base frequency portion and its integer multiples (harmonics). The so-called narrow band noise spectrum therefore shows only portions at discrete frequencies while in between showing the environmental noise.
- A non-periodical signal, such as a data-stream, consists of portions of all frequencies. This is called wide band noise.
- Typical spectra measurements of NEC microcontroller include a combination of both noise types as shown in the example.

Figure 2-1: Narrow band noise and wide band noise



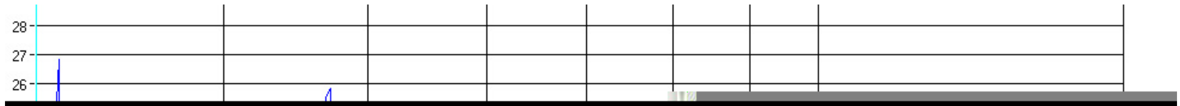
[redacted]

Remark: In the Figure 2-1, the wide band noise dominates the lower frequency range of the diagram, the narrow band noise dominates the upper frequency range of the diagram.

2.3.2 Power consumption of clocked CMOS circuits

Power consumption of CMOS circuits is mainly related to the switching frequency of the circuit. Even if a circuit additionally consumes DC-power this is not relevant for EMC.
The measurement in Figure 2-2 shows the power consumption of a CMOS circuit once operated at 2 MHz (red) and once at 8 MHz (blue). Obviously, roughly 4 times the frequency causes 4 times (or +12 dB) the power consumption.

Figure 2-2: CMOS power consumption versus frequency



[redacted]

2.3.3 Spectra of rectangular and trapeziodal signals

According to Fourier, the AC-spectrum of a rectangular signal with 50% duty cycle is composed of the base frequency and its harmonics as per the following formula [3]:

$$\text{Signal} = A \times \sum_{n=1}^{\infty} \frac{\sin(n \times \omega t)}{n}$$

with n = 1, 3, 5, …

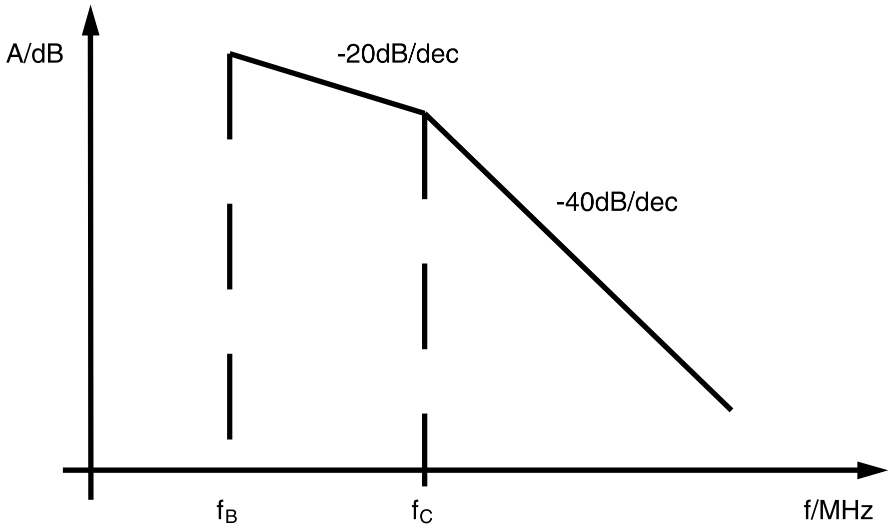
Obviously, the amplitude diminishes by 1/n or –20 dB per decade.
For comparison with measurements the peak-to-peak Amplitude has to be corrected to root-mean-square (RMS) as this is typically measured by a spectrum analyser etc.:

$$A_{RMS} = A_{PP} \times \frac{1}{2\sqrt{2}}$$

Fortunately, rectangular signals are only a limited view assuming 0 ns rise- and fall-time. Based on the assumption of equal rise- and fall-time a spectrum falls by –20 dB per decade up to a specific corner frequency. Above this frequency the spectrum falls with –40 dB per decade with a transition area in-between. The corner frequency [4] is given by:

$$f_C = \frac{1}{\pi t_R} = \frac{1}{\pi t_F}$$

Figure 2-3: Spectrum of a digital signal



Example:

Emission strength at 100 MHz for different clock signals

The signal strength of any 5 V clock signal at its base frequency is:

$$20 \times \log\frac{5\ \text{V}}{2\sqrt{2} \times 1\ \mu\text{V}} = 125\ \text{db}\mu\text{V}$$

If the signal is rectangular its strength decreases by 20 dB per frequency decade.

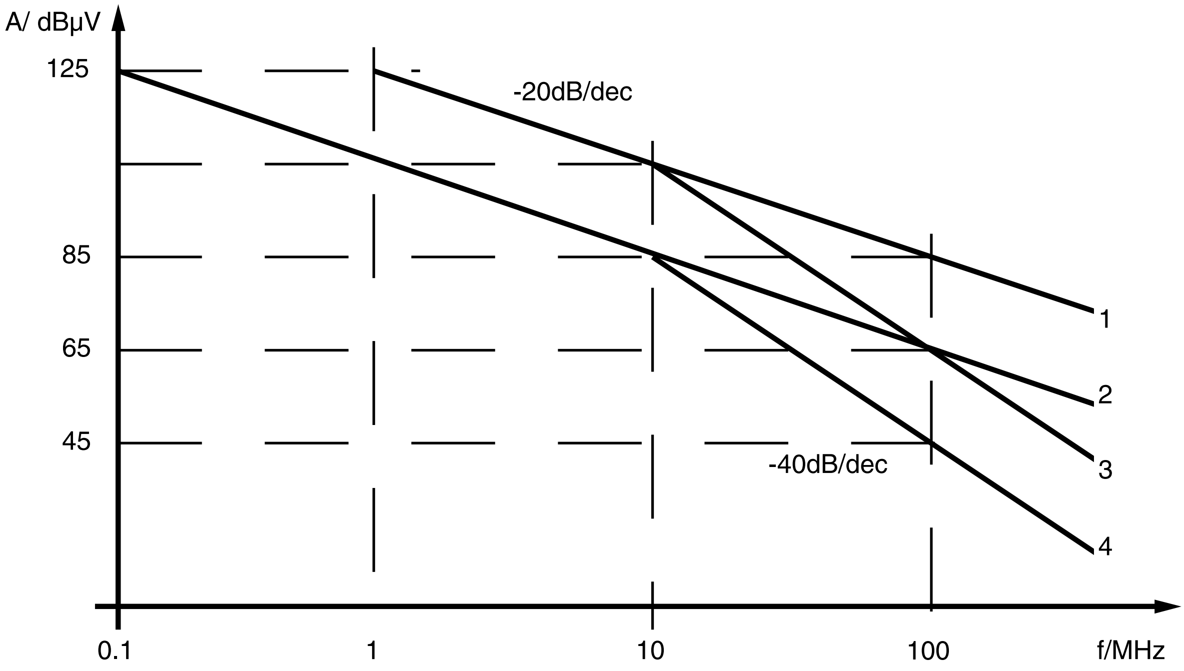
- Assumed its base frequency is 1 MHz, the observation frequency of 100 MHz is 2 decades higher and therefore the harmonic strength is about 40 dB lower. So the emission at 100 MHz is 85 dbµV (curve 1).
- Reducing the base frequency to 100 KHz reduces the emission at 100 MHz by 20 dB as 100 MHz is 3 decades higher than 100 KHz, the emission at 100 MHz is therefore only 65 dbµV (curve 2).

If the signal is trapeziodal with about 32 ns rise- and fall-time its corner frequency is 10 MHz. Up to 10 MHz the signal strength decreases by 20 dB per frequency decade. From 10 MHz onwards the signal strength decreases by 40 dB per frequency decade.

- Assumed again the signal base frequency is 1 MHz, at 10 MHz the emission is already 20 dB lower and at the observation frequency of 100 MHz it is another 40 dB lower. So the emission at 100 MHz is 65 dbµV (curve 1 until 10 MHz and curve 3).
- Reducing again the base frequency to 100 KHz reduces the emission at 100 MHz by another 20 dB and the emission at 100 MHz is therefore only 45 dbµV (curve 2 until 10 MHz and curve 4).

Figure 2-4 summarises the results.

Figure 2-4: Emission strength of rectangular and trapeziodal signals



2.4 Thumb Rules

2.4.1 There is only three counter measures to achieve EMC

Handling of currents and voltages is of course much easier than working on 3-dimensional electromagnetic fields. Basically the number of countermeasures can be reduced to three.

- Avoidance of unnecessary RF-noise

  In CMOS devices the switching circuits generate the noise. Reduction of for instance the switching frequency or the number of switching circuits reduces the power consumption and therefore the emission. Any reduction of power consumption is a reduction of emission. This could be for example low voltage operation or the usage of power reduction modes of the devices.

- Keeping RF-energy away from antenna structures

  As calculated in the last chapter, RF-energy is not a problem if the structures dealing with it are too small for acting as effective antennas. A decoupling capacity for example provides the RF-energy locally keeping most of the RF-current in a small loop between device and capacitor.

- Transforming RF-energy into heat

  Any resistive material such as resistors, ferrites etc. can be used for this measure.

2.4.2 Any piece of wire has an impedance

When discussing higher frequencies a wire is not longer just a connection. A wire has impedance caused by its self-inductance. As per [1] the self-inductance is in the range of 0.5nH/mm to 2.0nH/mm. For EMC the absolute value is not important but the acknowledgement and detailed contemplation of this impedance is of highest importance. According to

$$Z' = 2 \times \pi \times f \times L'$$

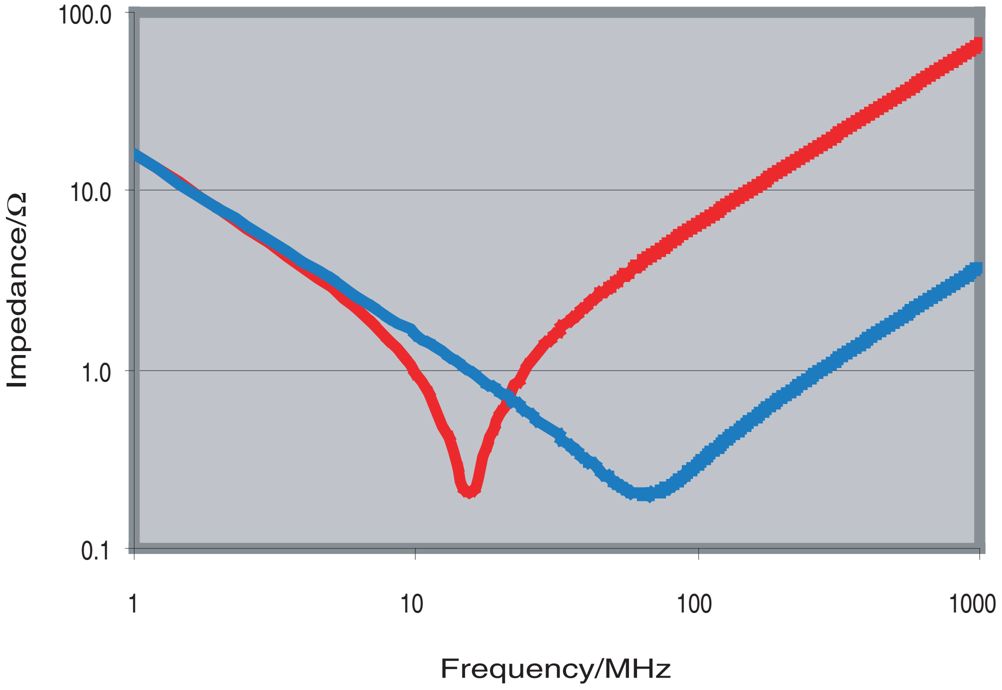
with L' = 1 nH/mm as a medium value the inductor impedance at for example 100 MHz is

$$Z' \approx 0.6\ \Omega/\text{mm}$$

Example:

The blue plot in Figure 2-5 shows the calculated impedance of a decoupling capacity of 10 nF in 0603 package (ESL = 0.6 nH) and X7R dielectric (ESR = 0.2 Ω). The red plot shows the same capacity but connected via 2 little stubs of “only” 5 mm each ($L = 2 \times 5$ nH).
Obviously, from a specific frequency onwards the distance between both curves is nearly constant. In this example from about 60 MHz onwards the “red impedance” is at least 17 times higher than the “blue impedance”. Further, the low impedant area of the series resonance has become much smaller and has moved to lower frequencies due to the trace inductance. Overall, the capacitors filter efficiency has suffered dramatically from the two “little” stubs.

Figure 2-5: Stub wire impedance influence



2.4.3 Linear versus logarithmic scale

In EMC huge dynamic ranges (µV to KV) have to be described. The logarithmic scale is preferably used when small values within a huge dynamic range shall be described. The logarithmic scale is a comparative scale and therefore always requires a reference value. It uses the artificial unit dB and is calculated as per following formula:

$$\text{Value/dB} = 20 \times \log \frac{\text{Value}}{\text{Reference}}$$

For specific reference values (µV, µV/m etc.) the reference is marked by using dB with suffix (dBµV, dBµV/m). If not marked the reference must be mentioned explicitly. Due to the nature of the logarithms the multiplication in linear scale is replaced by a summation in logarithmic scale. Therefore for estimation the terms as given in the table below are useful. For example the stub wires above increase the impedance by factor 17, which is approximately 16 or 2 × 2 × 2 × 2. In other words the impedance is increased by 6 dB + 6 dB + 6 dB + 6 dB or 24 dB compared to the minimum impedance.

Linear	Logarithmic
Factor 0.1	- 20 dB
Factor 0.5	- 6 dB
Factor 2	+ 6 dB
Factor 10	+ 20 dB
Factor 100	+ 40 dB
Factor 1000	+ 60 dB

2.4.4 Definition of frequency ranges

In this application note the definition of low, mid and high frequencies shall be handled in relation to the frequency response of major elements on PCB, such as decoupling capacities. Therefore the frequency ranges mentioned below are only for rough orientation.

- ‘Low’ are all frequencies at which the parasitic elements such as ESL or trace impedance can be neglected. This is typically the case for frequencies below up to about 30 MHz.
- ‘High’ are all frequencies at which the parasitic elements such as ESL or trace impedance must be considered. This is typically the case for frequencies from about 80 MHz onwards.
- ‘Medium’ are the frequencies in between.

[MEMO]

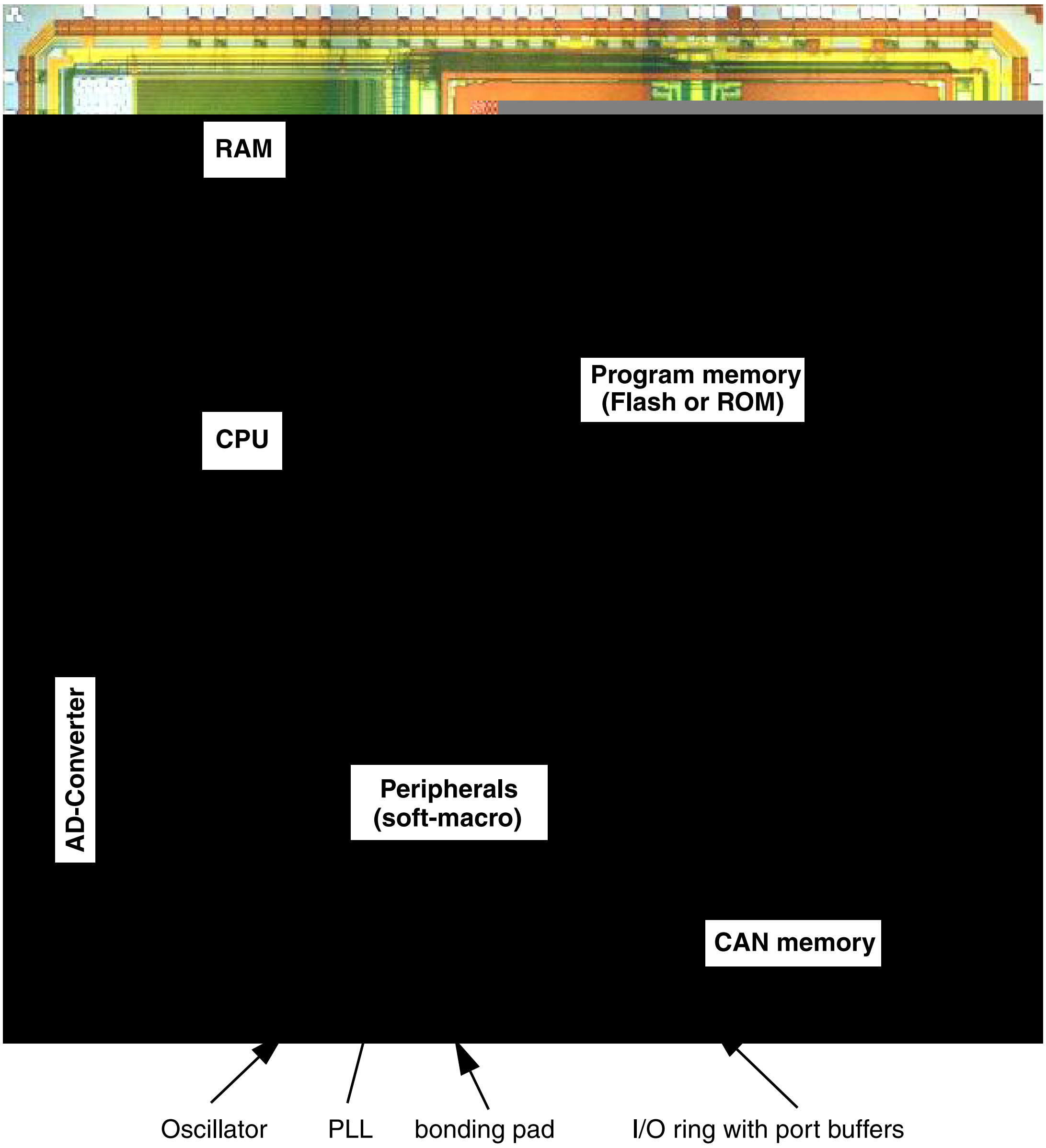
Chapter 3 NEC Microcontroller

The microcontroller portfolio of NEC includes general-purpose microcontroller families as well as microcontroller families especially designed for specific markets. For many years now NEC CMOS microcontroller incorporate a variety of EMC techniques. Some of these techniques are effective without any measure on customer side. Others require appropriate action on PCB-design side. Therefore it is necessary to understand major sources of noise inside a NEC CMOS microcontroller and its propagation to the outside.

3.1 A Typical Microcontroller Layout

In the following chapters details of semiconductors will be discussed. The technical terms shall be briefly explained by means of the following picture.

Figure 3-1: A typical microcontroller layout



All internal logic except AD-converter, oscillator and I/O-ring is identified as the core. Typically the core has no connection to pins except for its power pins. In the above picture for example the core contains the CPU, PLL, program memory, RAM and peripherals including CAN memory. The I/O-ring consists of the power and ground rail system with the port buffers and their protection circuits. The I/O-ring power supply of most NEC microcontroller is separated from the core power supply.

3.2 Major Noise Sources

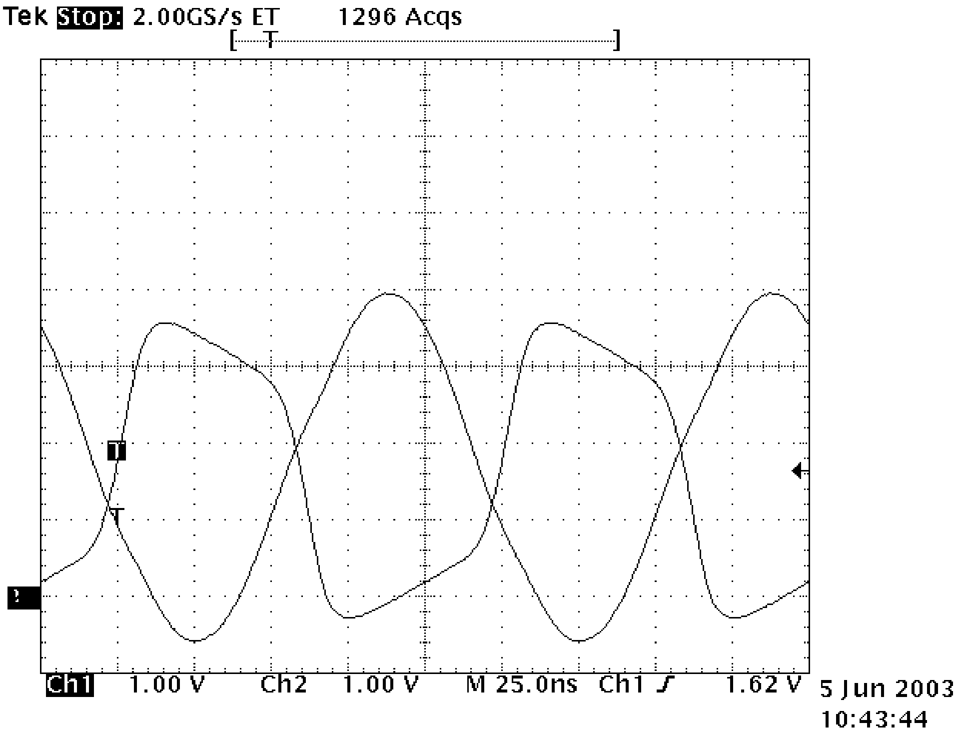
As per experience in NEC EE especially at higher frequencies the narrow band noise is higher than wide band noise. Therefore the following chapters will concentrate on narrow band noise.

3.2.1 Oscillator

When considering clocks and narrow band noise, naturally the oscillator comes into ones mind.
Figure 3-2 shows a typical measurement of the quartz oscillator signals X1 and X2 of a NEC microcontroller. Although the signal shape is not exactly sinusoidal it is obviously close to. In fact, according spectrum measurements show only few harmonics. Further, compared to the total power consumption of a microcontroller, the power consumption of the oscillator is rather low. Therefore the contribution of the quartz oscillator of a NEC microcontroller to the applications noise emission is rather low. Nevertheless, the signal shape and thus the spectrum may be much different for other types of oscillator, for example RC-oscillator.

Note: Although the quartz oscillator is not a big issue for emission it may be susceptible to noise. Therefore special care must be taken when routing the oscillator section of a microcontroller application.

Figure 3-2: Quartz oscillator signals X1 and X2



3.2.2 Core, PLL and clock-tree

Inside a digital device like a microcontroller a sinusoidal clock cannot be used. Therefore, in NEC's CMOS microcontroller the oscillator clock is rectangular reshaped and distributed inside the device via the clock-tree. For functional reasons the propagation delay into the various branches of the clock-tree must be tuned to provide the clock-edges all over the device at almost the same time. All switching core elements therefore draw current at almost the same time. The resulting pulsed core supply current is the major core related noise source. NEC microcontroller usually use both edges of the clock. The

3.3 Noise Propagation to Non-Switching Pins

Switching pins are very obvious noise sources. Unfortunately there are also other effects that lead to emission of ostensibly unconcerned pins. Some of these shall be described now.

3.3.1 Microcontroller supply system

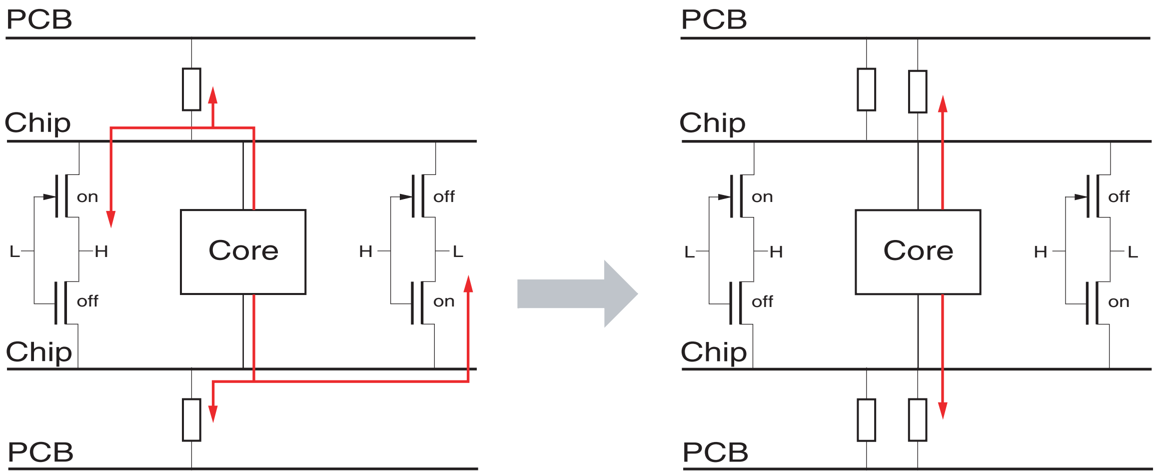
A supply system consists of one or more power pins and their related ground pins. Commonly, NEC microcontroller provide several separated power supply systems, which are separated from each other on power and ground side. At least one decoupling capacity for each power supply system is mandatory to provide the required power at low impedance over a wide frequency range.
Any active element inside a microcontroller has direct or indirect a connection to at least one power supply system. Thus, any switching inside the microcontroller causes a current to flow. The emission of this current is proportional to the area of the loop(s) in which the current flows. Hence, these loops have to be designed as small as possible. The most important example here is the current loop between microcontroller and decoupling capacity.
Any power supply has a source impedance higher than 0 Ohm, especially at higher frequencies when the inductive wire impedance becomes significant. Pulsed currents therefore overlay a ripple voltage to the DC power supply that contributes to the emission. Providing the power to the microcontroller at low impedance may reduce this emission.

3.3.2 Cross-talk of core noise to I/O-ports

(1) Common impedance coupling

Any two circuits sharing a common impedance in their power supply will suffer from cross-talk between each other. The left part of below figure illustrates the core-noise propagation in case of a common power supply for core and I/O-ring. The noise is caused by the core-current related voltage drop across the bond wire and pin inductance. In Figure 3-3 these are represented by the shown resistors. Even if the power supply system on PCB were to be free from any voltage ripple the chip-internal power supply would be noisy. As the port buffers and the core refer to the same internal power supply, the noise propagates to each output pin via the active transistor. But not only output pins, also input pins are affected due to parasitic capacities (for example protection circuits) inside the chip. With this configuration EME sensitive applications may require filtering of each pin. At least for microcontrollers with many pins this is for cost and space reasons seldom reasonable.

Figure 3-3: Cross-talk of common versus separated power supply



A separated power supply system for the core as illustrated in the right part of Figure 3-3 overcomes this coupling to a large extend. The separation should be made on both, power and ground side in order to avoid effectively the disadvantages of common impedance coupling. By means of that, the core related emission via the I/O-ports may be dramatically improved.

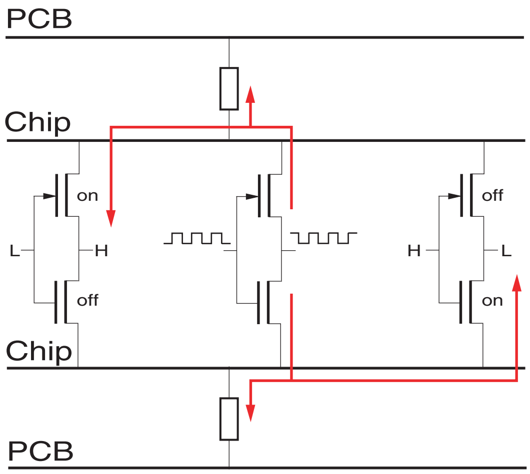
(2) Capacitive and inductive coupling

As per the experience in NEC EE, the common impedance coupling is the prevailing effect for cross-talk from core to I/O-ports. Nevertheless, capacitive and inductive coupling inside the chip and/or the package occurs as well. Due to rather high source impedance the capacitive coupling should not be a big issue. Inductive coupling occurs whenever a high frequency current flows beside another wire. On-chip this effect is minimised by means of optimised routing but the bonding can hardly be optimised as it is a highly aligned structure. Therefore comparably higher core related noise has to be expected on pins adjacent to core power or ground pins.

3.3.3 Cross-talk between I/O-ports

The cross-talk effect due to common impedance coupling as described above generally also occurs between I/O-ports. For obvious reasons not each and every I/O-port can be provided with a separate power supply system. Therefore the cross-talk effects can be minimised by chip design measures but not avoided. Possible countermeasures on application side are for example reduction of frequency or filtering of the most affected pins. As cross-talk to inputs usually is lower than to outputs also temporarily re-configuring of outputs to inputs (where possible) may help. Unnecessary switching should be avoided at all. For example if the system clock driver is not used (open pin) but active, the cross-talk to other I/O-ports may be too high to comply with fastidious EME requirements.

Figure 3-4: Cross-talk between I/O-ports



Chapter 4 Examples for On-Chip EMC Measures in NEC Microcontroller

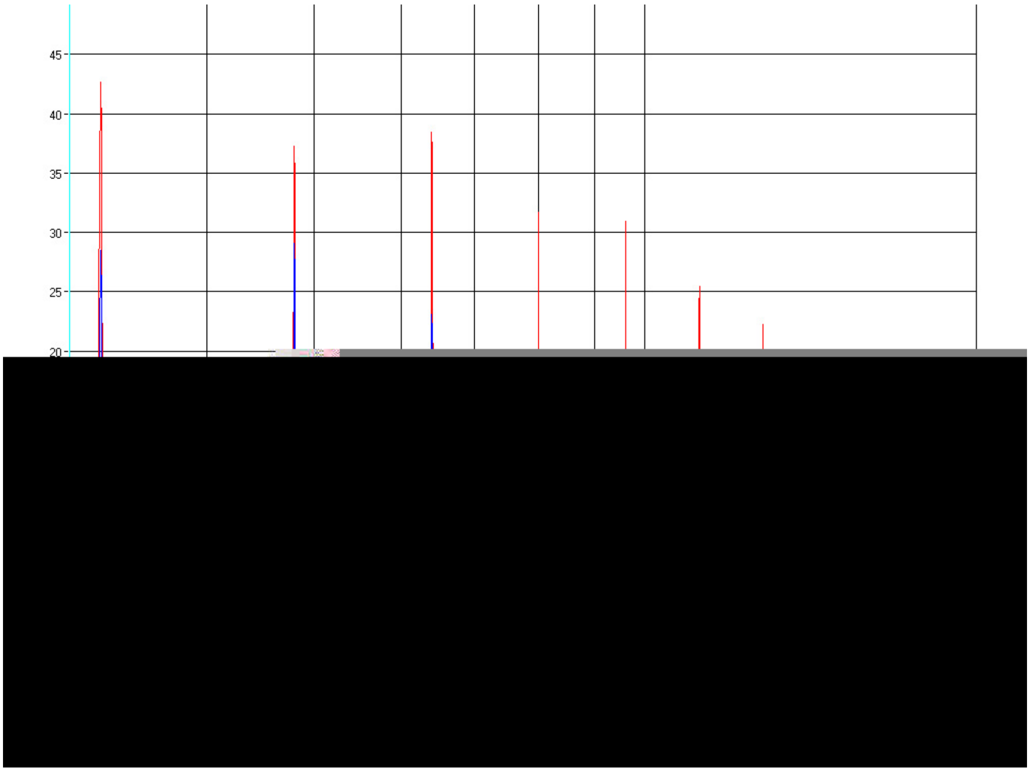
For many years now NEC CMOS microcontroller incorporate a variety of EMC techniques. On-chip capacities and spread spectrum clock generator, although effective without any measure on PCB design side, are described first. Further, as the application note focuses on PCB design techniques only few on-chip measures out of the NEC EMC portfolio are shown here. These are powerful measures for EMC, which should be considered during the selection phase for a microcontroller.

4.1 On-Chip Capacities

EME-optimised decoupling targets to provide a maximum of the required HF-current by one or more decoupling capacitor(s). The more HF-current is kept in the loop between the switching circuit on the chip and the capacitor the lower is the contamination of the remaining power supply circuit. For optimisation of the connecting line impedance usually the capacitor is located as near as possible to the supply pins of the microcontroller. For reduction of the current loop emission, the loop area should be minimised. By using only PCB-design techniques further significant improvements are difficult to achieve. Thus the consistent countermeasure is to move parts of the decoupling capacitor onto the chip thereby reducing the connecting impedance and the currents loop area considerably. These on-chip capacities are too small to provide the whole decoupling, so capacities on PCB are still necessary. Nevertheless, for the higher frequency range they may reduce the emission impressively.

The measurement results in Figure 4-1 compare the “same” microcontroller with and without on-chip capacities. The red plot shows the emission of the original version and the blue plot of the redesigned version with on-chip capacities. Over a wide frequency range improvements of up to about 15 dB have been achieved without increasing the chip size, means without adding extra cost.

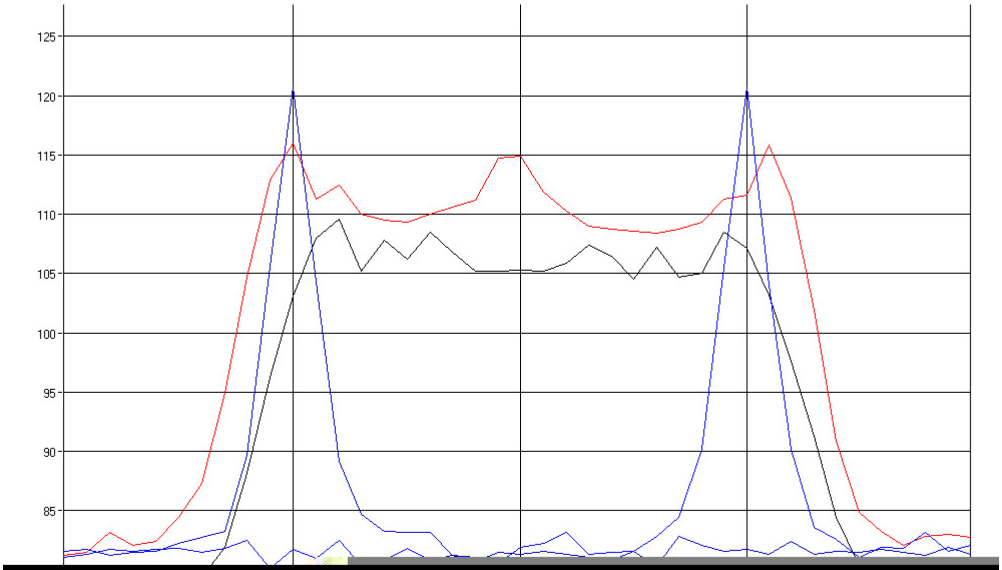
Figure 4-1: EME with on-chip capacities



4.2 Spread spectrum cock generator (SSCG)

As per the experience in NEC EE especially at higher frequencies the narrow band emission is dominant against the wide band emission. The nature of narrow band spectra is to show only portions at discrete frequencies while in between showing the environmental noise. Unfortunately, if only one peak is above the limit the application fails the test although wide frequency areas may show big distance to the limit. By modulating the CPU operation frequency the HF-energy is spread over a wider frequency range thereby reducing the peak energy. The blue measurement results in Figure 4-2 show the emission peaks of static frequencies. The red plot shows the modulated spectrum measured with a peak detector while the black plot was measured with a quasi-peak detector. With a modulation of only about ± 1% the peak emission was reduced up to about 10 dB by distributing the HF-energy over 2 MHz bandwidth. Further improvements can be achieved by increasing the modulation width.

Figure 4-2: EME with SSCG



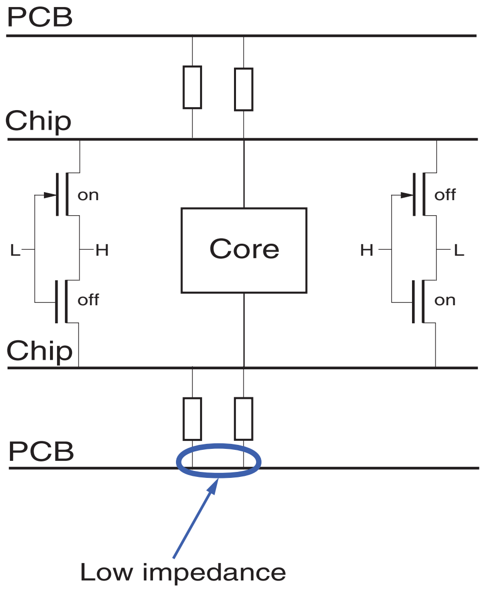
[redacted]

4.3 Multiple Separated Power Supplies

In NEC microcontroller the power supply separation is widely used to effectively reduce cross-talk between core and I/O-ports. Further analogue circuits, clock generation and sometimes the external bus interface may be supplied separately. For gaining the maximum improvement the separation is usually made on power- and ground-side although this causes considerably higher efforts for internal ESD protection. Beside protection efforts the utilisation of this measure is further limited by the availability of pins, especially in small packages with low pin-count. On the other hand, devices with high pin-count may have multiple supply pins for the same supply system in order to reduce the connecting impedance between PCB and on-chip supply system.

Required action on PCB design side:
Although being separated in the power supply of course there are some internal control signals between core and I/O-driver or any other separated circuit. In order to keep both supply systems on a similar potential both grounds must be connected with each other on the PCB via low impedance.

Figure 4-3: Ground impedance consideration

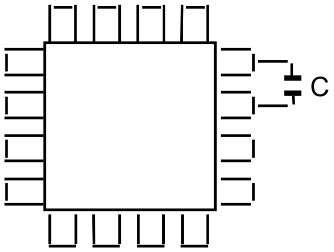


4.4 Adjacent Power and Ground Pins

By far the majority of NEC microcontroller are equipped with adjacent power supply pins. This pinout allows the PCB designer to easily minimise the current loop size between microcontroller and decoupling capacity. Minimisation of the loop size of course requires one capacity each per adjacent supply pair. Concurrently, reduction of the loop size also reduces the connecting impedance of the decoupling capacity.

Required action on PCB design side:
Move the decoupling capacities as near as possible to the supply pins. Treat each piece of wire like an impedance. Especially the connection of the decoupling circuit with the board power supply system should be carefully considered.

Figure 4-4: Adjacent power pining



Remark: Listed above are only few of today’s possible on-chip EMC measures. As per common understanding, measures to achieve EMC are the more effective the nearer to the source of the noise these are applied and the earlier in the design process these are taken into account. Problems on EMC identified at late stage during application tests not only cause high cost for their correction but sometimes also delay market introduction of the whole application. Further, at that stage several substantial decisions such as device selection have been made. Thus consider LSI-level EMC measurements prior to selecting a new microcontroller for the next project.

Note: IEC 61967-x is a suitable family of test standards for chip-level EME measurements. NEC provides measurement reports of almost all microcontroller device families according to IEC 61967-4. Please contact your local NEC sales representative to get a copy of a specific measurement report.

Chapter 5 Examples for PCB-Design Measures for Improved EMC of NEC Microcontroller

5.1 Power Supply Optimisation

The power supply system of a PCB usually consists of a ground system and one or more power supplies. Power and ground nets are usually the most distributed nets in the circuit, thereby unfortunately providing a suitable antenna for the microcontroller supply noise. It is therefore inevitable to carefully design the power supply circuit. The first step to achieve an optimised power supply design is to analyse the distortion potential of any device power and ground pin as considered above. PCB-design should always start with the routing of the power supply system.

5.1.1 Ground system

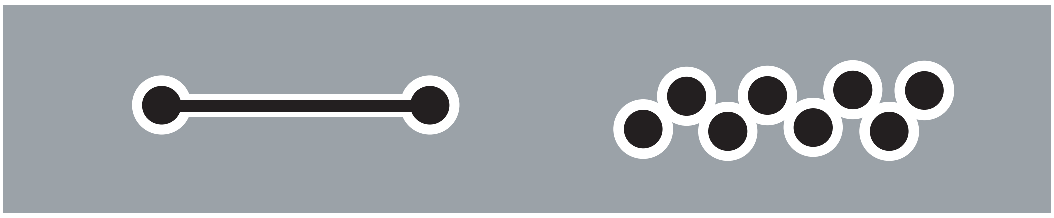
(1) System ground

The system ground has two major functions: On one side it is part of the power supply system and on the other hand it provides the reference level for all signals. According to Ohm's law any supply current in the ground system will cause a voltage drop proportional to the ground impedance. Due to the common used ground impedance (compare to section (1)"Common impedance coupling" on page 24) this voltage overlays all signals referring to this ground.
For optimisation the ground should have the lowest possible impedance and the noise current in the system ground should be minimised.

(2) Ground plane

In a multilayer PCB the first requirement can be fulfilled by utilising a complete layer as a ground plane. The ground layer must be free from any signal traces or other gaps longer than 10mm. Any gap in the ground increases its impedance and introduces so-called slot-antennas. Examples of unwanted slots are shown in Figure 5-1.

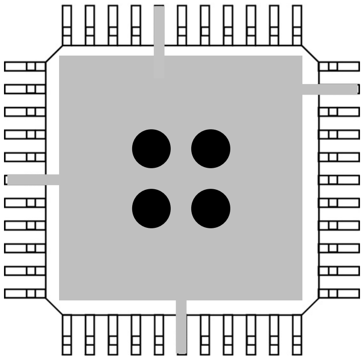
Figure 5-1: Slot Antennas



(3) Local device ground

The second requirement can be served by providing an extra local device ground below the device. This local device ground shall be connected by low impedance to the system ground in its centre as shown. By means of this structure local HF-currents are kept away from the system ground thereby avoiding related voltage drops in the system ground. The 4 connections to system ground as shown in Figure 5-2 are a compromise between low impedance (1/4th the impedance of only one connection) and minimum parallel connection between both grounds.

Figure 5-2: Local device ground



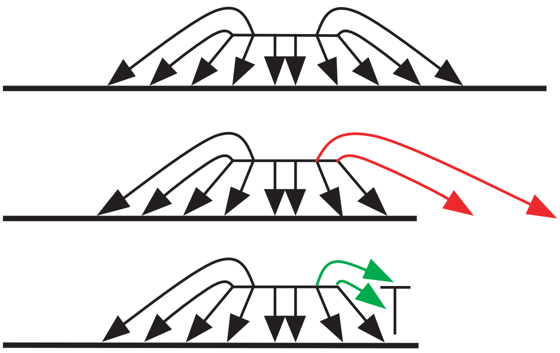
(4) Ground fill

Usually not every area on every layer is used for wiring. These unused areas should be filled with copper and then shall be connected to ground. It is not sufficient to connect these ground fills just “somewhere” to the ground plane. These ground fills shall be connected to ground in a grid at least every 10 mm. This measure further reduces the ground impedance and concomitantly reduces the cross-talk between layers.

(5) Guard ring on PCB-edges

The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. As shown in Figure 5-3 the field lines of the signal return to PCB-ground as long as an “infinite” ground is available. Traces near the PCB-edges do not have this “infinite” ground and therefore may radiate more than others. Thus signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or - if not avoidable – should be accompanied by a guard ring on the PCB edge.

Figure 5-3: Field lines of a signal above ground



The intention of the guard ring is that HF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 5-4. As these traces should have the same (HF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

Figure 5-4: Guard ring in a 4-layer PCB

5.1.2 Power routing and decoupling

After a reliable and low impedant ground was established the next step in PCB-design is the power routing.

(1) Power plane versus routed power traces

In multilayer PCB’s often one entire layer is used as a power plane. Other design methods comprise routed power traces or a combination of both techniques. The following shall oppose some advantages and disadvantages of both techniques.

Advantages of power planes

- Easy and fast to implement
- Low inductive power supply
- Creates a capacity together with ground plane

Disadvantages of power planes

- Requires one plane per supply system
- Increases cross-talk between different supply systems if these are not separated by a ground plane
- Due to low impedance distributes noise from one source into the whole supply system
- Tempts the PCB-designer to less careful power design

Advantages of routed power supplies

- Allows the usage of one layer for more than one supply system, thereby reducing the cross-talk between these supplies
- May reduce cross-talk within each supply system

Disadvantages of routed power supplies

- Requires more careful power routing
- Higher supply impedance may require extra capacity for supply stabilisation
- Considerable DC-resistance in case of high current

The optimum obviously is to apply the advantages of both methods. Therefore several local power planes should be implemented and connected to the supply via traces. Planes of different supply systems should be located in the same layer or separated by a ground plane to minimise cross-talk between these systems. Although the local power planes are easy to implement special care must be taken when connecting the power pins and the decoupling capacities to the planes.

(a) Connection of decoupling capacities

The decoupling of the most critical power supply pins of the microcontroller (for identification of these refer to chapter 3) very often is the most fastidious part in a PCB design. Even in a multilayer design every millimetre of trace has to be carefully considered.

(b) Sketch equivalent circuits

A piece of paper and a pencil are still useful tools. When considering the best placement, direction and connection of the capacity a small sketch may be very useful. Each piece of wire shall be drawn as an impedance even though the actual value is not important. The Figure 5-5 clearly indicates that the 2 red impedances should be minimised while the other 2 may be object to concessions.

Figure 5-5: Decoupling equivalent circuit

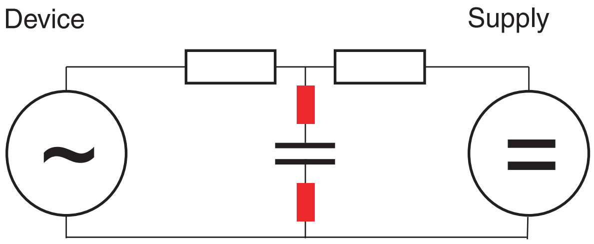
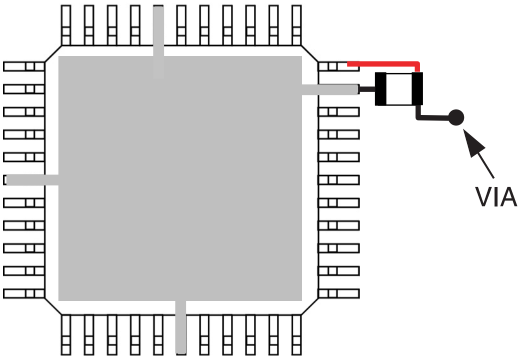


Figure 5-6 shows the implementation in the PCB-layout. The connection to the local ground plane has been kept as short as feasible. The power trace is routed from the device via the capacity pad to a VIA (through hole connection), which connects it to the inner power plane.
Placing the VIA for example in the centre of the red trace would have added several nH to the capacitors impedance and thereby would have reduced the filter efficiency tremendously.
Further, no power for other pins and/or devices must be fetched from the red trace, as it is very noisy.

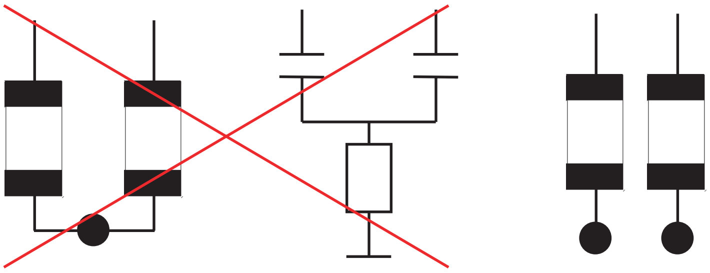
Figure 5-6: Decoupling PCB-layout



(2) A VIA has a considerable impedance

As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The 2 left parts of Figure 5-7 indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.

Figure 5-7: Cross-talk due to a shared VIA



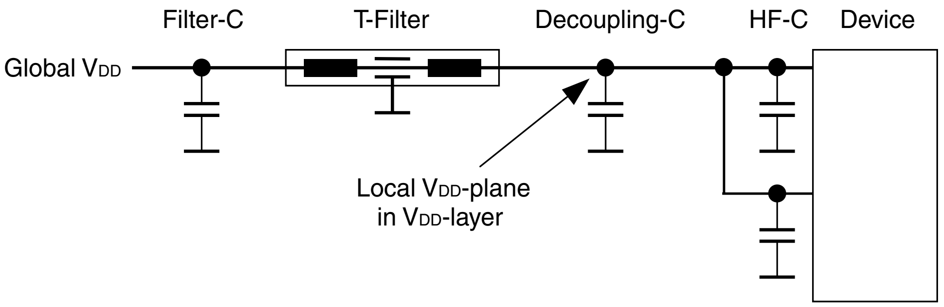
(3) Filter

When the above described design techniques are followed most applications should comply with their EMC requirements. Nevertheless, in case of critical EMC requirements or complex designs further filter elements may be necessary. In NEC EE good experience was made with a multiple stage power supply filter.

(a) Multiple stage power supply filter

The most critical power supplies should be filtered in multiple stages to achieve the maximum possible noise suppression. An example filter circuit is given below. As outlined before the impedance of each piece of wire has to be considered. Especially the connections of the vertical elements (in the example: all capacities) are critical. The T-filter for example provides a perfect connection of the power-line to the capacity without adding extra impedance. Only if the PCB design provides a comparably low impedant connection to ground the full suppression can be achieved.

Figure 5-8: Multiple stage power supply filter



HF-C:	For inductance minimization the smallest feasible package (0603 or smaller) should be used. Ceramic material NPO or at least X7R shall be used. The capacity value has to be evaluated during EMC tests. Start value should be the maximum available capacity in the chosen package. The connection to the device shall be implemented as described in chapter 5.1.2 "Power routing and decoupling" on page 33.
Decoupling-C:	This capacity provides medium frequency current to the device as it forms the pulsed device current into average "DC"-current. Its main task is to keep the power supply within DC-specification (e.g. 1.5 V +- 5%). One or more decoupling capacity (47 nF to 100 nF, X7R, 0603) shall be connected to the local V_{DD}-plane. The required capacity shall be calculated according to below formula, several capacities in parallel may be required in order to reduce the ripple caused by ESR and ESL.

$$C = \frac{I \times T}{U}$$

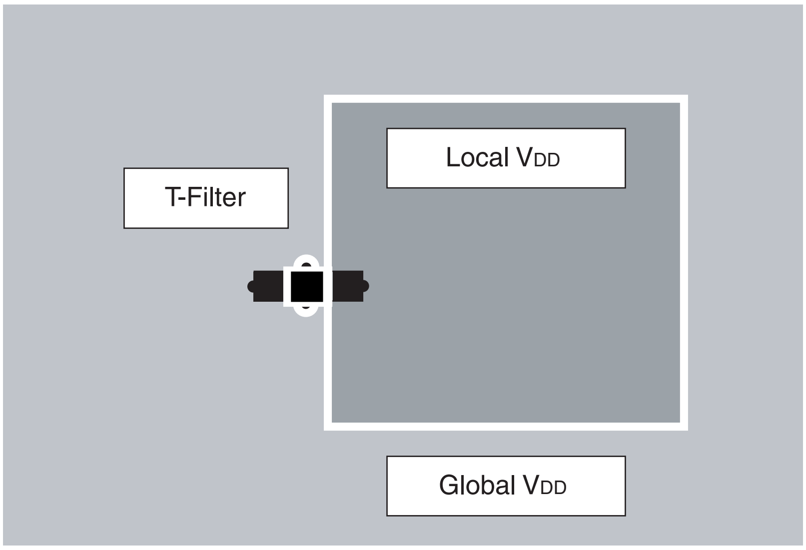
with I = maximum average current for the supply-system
with T = operating clock period
with U = acceptable voltage ripple, default is 1%

Example:

For a 3.3 V supply system the acceptable voltage ripple is U=33 mV. With a quartz of 8 MHz and a 5-times PLL the operating frequency is 40 MHz or T=25 ns. If the average device current in the supply system to be decoupled is I=100 mA the decoupling capacity has to be at least 76 nF.
The so calculated decoupling capacity may be reduced by the accumulated value of all HF-capacities as these are for medium frequencies in parallel. The connections to the ground plane and to the local V_{DD}-plane shall be made by at least 2 VIAs each. If the production constraints allow, the VIAs shall be placed within the soldering pads, otherwise the shortest possible trace-length (max. 1 mm) shall be used for connection.

T-Filter: The ferrite T-Filter (e.g. Murata NFM60R30T222) separates the local V_{DD}-plane from global V_{DD}. It keeps the antenna for the device supply current noise small and transforms HF-energy into heat.
The ground connection is most critical and shall be made by at least 2 VIAs. If the production constraints allow, the VIAs shall be placed within the soldering pad of the filter, otherwise the shortest possible trace-length (max. 1 mm) shall be used for the ground connection.

Figure 5-9: Local V_{DD} separated by T-Filter

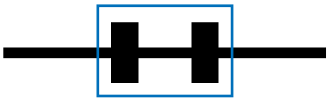


Filter-C: This filter capacity (47 nF to 100 nF, X7R, 0603) forms another LRC-Filter with the 1st half of the ferrite filter.

(b) Spare bridging elements

In case the distortion potential of a power supply is not clear the best possible filtering should be implemented with the option to omit parts that according to later evaluation may not be needed. Parallel parts are easy to omit but serial parts require an optional bridging element, for example as shown in Figure 5-10. If later tests prove the necessity of the serial element no other parts have to be moved to find a place for the new element. On the other hand, not too much extra elements should be provided as these may cause space restriction for other parts of the circuit.

Figure 5-10: Spare bridging element



5.2 Signal Routing

Before starting the PCB-design the circuit should be analysed for critical signals according to the background as described for example in this application note. For most critical signals such as clocks, strobes and other often switching signals one or more of the following measures should be applied.

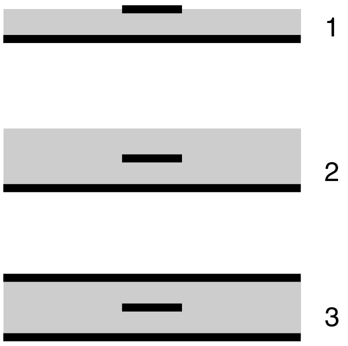
5.2.1 Line termination

According to [5] circuit designers can choose from many different termination techniques. Line termination may be necessary on long traces to avoid reflections or on short traces to avoid ringing. Most common are end- or source-terminations. End-terminations for example minimise the rise time of the signal and therefore may be suitable for speed optimisation. Source- or series-terminations minimise the current on the signal trace and therefore are preferable for emission reduction.
The resistor for series termination has to be located as near as possible to the driver (source) of the signal. It may be optimised to match the transmission line impedance or to create a low pass filter with the load capacitance. If the transmission line impedance shall be matched the sum of driver impedance and resistor value has to be equal to the transmission line impedance. For EME-optimisation the current on the signal trace and the harmonics of the signal frequency should be minimised. Therefore a resistor value as high as the timing and functional constraints allow is desirable here.

5.2.2 Transmission lines on PCBs

The most common transmission lines used on PCBs are either strip line or microstrip line geometries. More or less complex and accurate formulas for the calculation of impedance, delay etc. are available in [5]. In Figure 5-11 drawings 1 and 2 are examples for microstrip lines; drawing 3 is an example for a strip line geometry. It is important to note that the calculation of strip line or microstrip line parameters presumes infinite ground. As this is not realisable the ground plane on either side of the signal trace should be at least 5 times wider than the maximum of signal-trace-width and signal-trace-distance to ground. This requirement is another reason for implementing the guard ring as it allows to route traces near the board edges.
When implementing strip lines or microstrip lines in a PCB-design make sure that above presumption is met by the design. Any crossing of other traces locally modifies the characteristic of the strip line or microstrip line and may cause inadvertently higher emissions. Also the power plane is not suitable as reference plane for a strip line or microstrip line.

Figure 5-11: Microstrip and strip line geometries

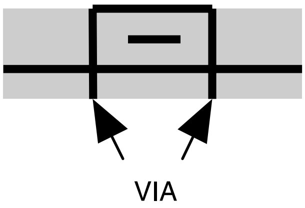


5.2.3 Layer stacking

The layer stacking, i.e. the distances between all layers of the PCB, should be carefully considered and defined. The distance to ground and the thickness of the surrounding material influences the characteristic of all traces. Further the emission of a signal above ground is somehow proportional to its distance from ground. Therefore the maximum height of any critical signal above ground should not be more than 0.2 mm. Clocks of frequencies higher than 30 MHz should not be farther from ground than 0.1 mm. Clocks of frequencies higher than 50 MHz should be routed as a strip line.

If only very few strip lines are required the second ground plane can be avoided by covering these signals with ground. For that purpose the clock signal is routed on a layer adjacent to the ground layer. On the next layer a wider ground trace is routed on top of the clock signal. This ground trace is connected to the ground plane on both sides of the clock signal every 5-10 mm. The Figure 5-12 gives an example for a 4-layer PCB.

Figure 5-12: Covered signal line



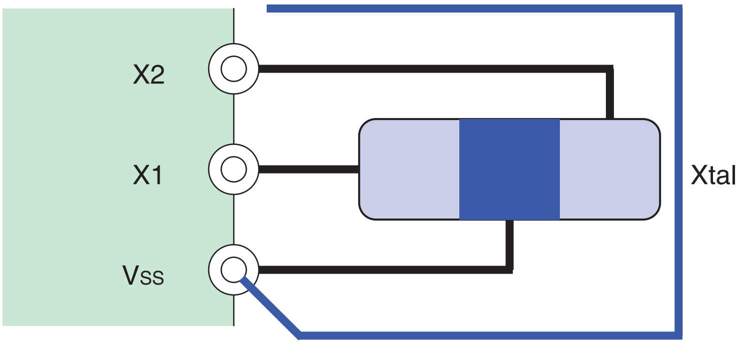
5.3 Oscillator

User's manuals of NEC microcontroller usually contain a chapter on the oscillator and its allowable and not-allowable wiring. Make sure to read this chapter prior to designing the clock circuit of your PCB.

5.3.1 Optimised pinout

Quartz oscillators in NEC microcontroller usually are optimise for the intended frequency range and therefore should not be critical for emission. Nevertheless, NEC microcontroller commonly provide an oscillator pinout that allows short connections between quartz and microcontroller as shown in Figure 5-13. Further, the adjacent ground pin allows to easily implement a special guard ring around the oscillator circuit.

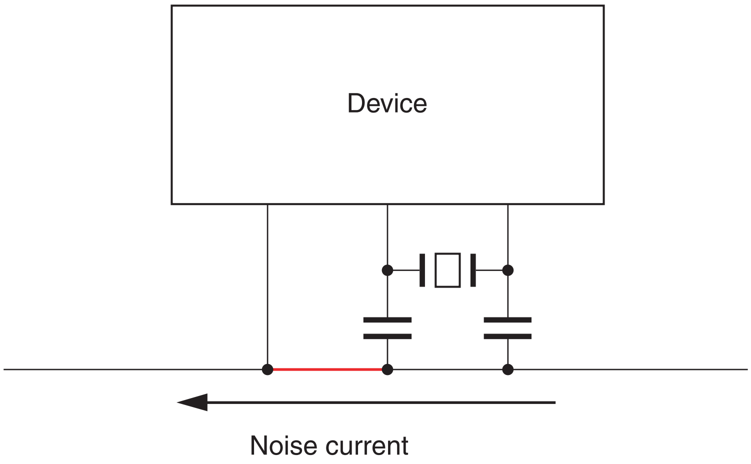
Figure 5-13: Optimised oscillator pinout



5.3.2 Oscillator ground connection

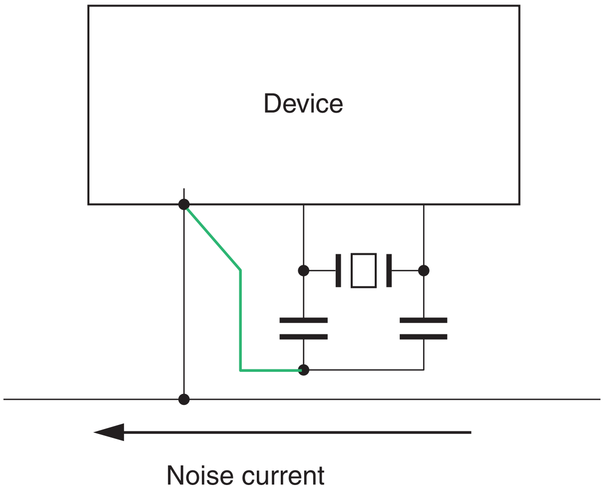
Although the impedance of a ground plane is low it is of course not zero. Therefore any noise current in the ground plane causes a voltage drop in the ground. If the 2 capacities of the oscillator are connected directly to the ground plane the voltage drop in the red portion of the ground in Figure 5-14 will be overlaid to the oscillator signals. If the noise related voltage drop is big enough the oscillator may be disturbed.

Figure 5-14: Poor oscillator ground connection



The overlay of ground noise may be avoided by providing an extra ground trace for the oscillator ground as indicated in green in Figure 5-15. This is even in a multilayer PCB a powerful measure to improve the susceptibility of the oscillator.

Figure 5-15: Optimised oscillator ground connection



Chapter 6 Items to Remember

1. Direct semiconductor contribution to the far field emission can be neglected, as on-chip structures are too small for being an effective antenna. The microcontroller generates currents and voltages, which stimulate the PCB layout and the connected cables. The PCB and the connected wiring harness act as antenna structures in both directions (EME and EMS) EMC of microcontroller devices is therefore mainly an issue of current, voltage and impedance.

2. Any piece of wire has an inductance that gets a remarkable impedance with increasing frequency. Especially in filter circuits any wire impedance must be considered.

3. Especially at higher frequencies the narrow band noise usually is dominant against the wide band noise. Emission related to the device operation frequency is mainly emitted by the supply- and ground-current of the core while the noise contribution of the oscillator is rather low. The most critical signal of the external memory interface is the system- and/or memory-clock driver.

4. Frequently switching IO-signals, especially repetitive signals have to be considered to significantly contribute to the applications emission. The system clock driver should not be enabled for EME-sensitive applications.

5. The maximum height of any critical signal above ground should not be more than 0.2 mm. Clocks of frequencies higher than 30 MHz should not be farther from ground than 0.1 mm. Clocks of frequencies higher than 50 MHz should be routed as a strip line or as covered signal line.

[MEMO]

Chapter 7 Literature

[1]	Durcansky	EMV-gerechtes Geräte design
[2]	AVX	AVX capacity calculation software SpiCap (**http://www.avx.com**)
[3]	Bronstein-Semendjajew	Taschenbuch der Mathematik
[4]	IEC 61967-4	Integrated circuits - Measurement of electromagnetic emissions, 150 KHz to 1 GHz - Part 4: Measurement of conducted emissions – 1 Ω / 150 Ω direct coupling method
[5]	Howard Johnson Martin Graham	High speed digital design, A handbook of black magic

[MEMO]

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